WHAT IS CLAIMED AS NEW AND DESIRED TO BE PROTECTED BY LETTERS PATENT IS:

1. A method of fabricating a semiconductor device, comprising:

forming an emitter region;

forming a base region; and

forming a collector region symmetrically self-aligned with said emitter region.

2. A method as recited in claim 1, comprising:

forming a plurality of layers including an emitter layer, a base layer and a collector layer; and

etching said layers to form a vertical structure having said emitter region, base region and a collector region with substantially the same width.

3. A method as recited in claim 2, comprising:

etching said emitter region to form an emitter portion having a width less than a width of said emitter region and being self-centered with said base region and to form a base metalization area; and

forming contacts to said emitter region, said collector layer and said base metalization area.

4. A method as recited in claim 2, comprising:

etching said emitter region to form an emitter portion having a width less than a width of said emitter region and being self-centered with said base region; and

etching said collector region to form a collector portion having a width less than a width of said collector region and being self-centered with said base region and symmetric with said emitter portion.

5. A method as recited in claim 4, comprising:

forming said emitter portion from an emitter side of said device; and

forming said collector portion from a collector side of said device.

6. A method as recited in claim 4, comprising:

forming said emitter portion and said collector portion using processing from only one side of said device.

7. A method as recited in claim 4, comprising:

forming said vertical structure using anisotropic etching; and

forming said emitter portion and said collector portion using selective etching.

8. A method as recited in claim 4, comprising:

anisotropically etching said layers to form said emitter region and expose said base layer;

selectively etching said emitter region to form first base ledges;

anisotropically etching said layers to form said collector region; and

selectively etching said collector region to form second base ledges.

9. A method as recited in claim 8, comprising:

performing said selectively etching steps to produce a collector region having a width wider than that of said emitter region.

10. A method as recited in claim 1, comprising:

forming a plurality of layers on a substrate;

forming said emitter region from one of said layers and forming a contact to said emitter region using processing on a front side of said substrate;

forming said collector region from another one of said layers using processing on said front side of said substrate; and

forming a contact to said collector region using processing from a back side of said device.

11. A method as recited in claim 10, comprising:

forming a removable material over said emitter layer;

attaching a second substrate to said removable material; and

removing said substrate to expose said collector region.

12. A method as recited in claim 2, comprising:

etching said collector region to have a desired width less than a width of said base region and greater than a width of said emitter region.

13. A method as recited in claim 1, comprising:

forming said regions on a first substrate;

depositing a removable film over said regions;

attaching a second substrate to said film; and

removing said first substrate to expose said collector region.

14. A method as recited in claim 13, wherein forming said collector region comprises:

etching said collector region after removing said first substrate to form a collector portion having a width less than a width of said base region and being self-centered with said base region..

15. A method as recited in claim 13, wherein forming said collector region comprises:

etching said collector region after removing said substrate to have a width less than a width of a base region and greater than a width of said emitter region.

16. A method as recited in claim 1, comprising:

forming an emitter mesa;

forming a sidewall on said emitter mesa;

repeating said step of forming a sidewall to form a thicker sidewall on said emitter mesa; and

forming said base region and said collector region to have substantially the same width using said thicker sidewall as a mask;

said emitter mesa being self-centered with said base region.

17. A method as recited in claim 16, comprising:

forming said regions on a first substrate;

depositing a removable film over said regions;

attaching a second substrate to said film; and

removing said first substrate to expose said collector region.

18. A method as recited in claim 16, comprising:

etching said collector region after removing said substrate to form a collector portion having a width less than a width of said base region and being self-centered with said base region.

19. A method as recited in claim 16, comprising:

etching said collector region after removing said substrate to have a width less than a width of a base region and greater than a width of said emitter region.

20. A method according to claim 1, comprising:

forming a heterojunction bipolar transistor emitter, base and collector regions;

forming said emitter region symmetrically self-aligned to said collector region;

forming said emitter region self-centered to said base region; and

forming said collector region self-centered to said base region.

21. A method as recited in claim 1, comprising:

forming said collector region self-centered with said base region.

22. A method of fabricating a semiconductor device, comprising:

forming a plurality of stacked layers;

forming a first active region from one of said layers;

forming a second active region separated from said first active region by a third active layer; and

forming said first and second active regions to be symmetrically self-aligned.

23. A method as recited in claim 22, comprising:

forming said first and second active regions to be self-centered with said third active region.

24. A method as recited in claim 22, comprising:

forming said first active region from one of said layers and forming a contact to said emitter region using processing on one side of said stacked layers;

forming said second active region from another one of said layers using processing on said one side of said stacked layers; and

forming a contact to said second active region using processing from a second side of said stacked layers.

25. A method as recited in claim 22, comprising:

forming a removable material over said stacked layers;

attaching a substrate to said removable material; and

removing said substrate to expose said second active region.

26. A method as recited in claim 22, comprising:

forming a third active region from said third active layer;

etching said second active region to have a desired width less than a width of said third active region and greater than a width of said first active region.

27. A method as recited in claim 22, comprising:

forming said layers on a first substrate;

depositing a removable film over said regions;

attaching a second substrate to said film; and

removing said first substrate to expose said second active region.

28. A method as recited in claim 22, comprising:

forming a third active region from said third active layer;

symmetrically self-aligning said first, second and third active regions using processing on only one side of said stacked layers.

29. A method as recited in claim 22, comprising:

forming a third active region from said third active layer;

symmetrically self-aligning said first, second and third active regions using processing on only a top side of said stacked layers;

forming a first portion in said first active region having a width less that a width of said first active region self-centered with respect to said third active region using processing on said front said of said stacked layers; and

forming a second portion in said second active region having a width less than a width of said second active region self-centered with respect to said third active region using processing from a back side of said stacked layers.

30. A method as recited in claim 22, comprising:

forming said first and second active regions using processing from only one side of said device.

31. A method as recited in claim 22, comprising:

etching said layers to form a vertical structure having first, second and third regions

with substantially the same width on a front said of said stacked layers;

forming a first portion in said first active region having a width less that a width of said first active region self-centered with respect to said third active region using processing on said front said of said stacked layers; and

forming a second portion in said second active region having a width less than a width of said second active region self-centered with respect to said third active region using processing from said front side of said stacked layers.

32. A method as recited in claim 31, comprising:

anisotropically etching said layers to form a vertical structure having first, second and third regions with substantially the same width on a front said of said stacked layers; and

forming said first and second portions using selective etching.

33. A method as recited in claim 31, comprising:

anisotropically etching said layers to form said first active region and expose said third active region;

selectively etching said first active region to form first ledges in said third active region;

anisotropically etching said layers to form said second active region; and

selectively etching said second active region to form second ledges in said third active region.

34. A method as recited in claim 33, comprising:

performing said selectively etching steps to produce said second active region having a width wider than that of said first active region.

35. A method as recited in claim 22, comprising:

forming a vertical heterojunction field effect transistor.

36. A method of manufacturing a semiconductor device, comprising:

forming a plurality of layers including a collector layer, a base layer and an emitter layer on a substrate;

symmetrically self-aligning said collector layer, base layer and said emitter layer using processing on only one side of said substrate.

37. A method as recited in claim 36, comprising:

forming an emitter region in said emitter layer self-centered with respect to said base region.

38. A method as recited in claim 36, comprising:

forming a collector region in said collector layer self-centered with respect to said base region using processing from a front side of said substrate; and

forming a contact to said collector region using processing from a back side of said substrate.

39. A method as recited in claim 36, comprising:

symmetrically self-aligning said collector layer, base layer and said emitter layer using processing on only a front side of said substrate;

forming an emitter region in said emitter layer self-centered with respect to said base region using processing on said front said of said substrate; and

forming a collector region in said collector layer self-centered with respect to said base region using processing from a back side of said substrate.

40. A semiconductor device, comprising:

a first active region;

a second active region; and

a third active region disposed between said first and second active regions;

said first and second active regions being symmetrically self-aligned.

41. A device as recited in claim 40, comprising:

one of said first and second active regions being self-centered with said third active region.

42. A device as recited in claim 40, wherein:

said first active region comprises an emitter;

said second active region comprises a collector;

said third active region comprises a base; and

said collector is symmetrically self-aligned with said emitter;

43. A device as recited in claim 42, comprising:

one of said collector and said emitter being self-centered with said base.

44. A device as recited in claim 42, comprising:

said emitter having a narrow portion self-centered with said base; and

said collector having a narrow portion self-centered with said base and symmetric with said emitter portion.

45. A device as recited in claim 42, comprising:

said base having a lower and an upper ledge;

a first base contact formed on said upper ledge self-aligned with said emitter; and

a second base contact formed on said lower ledge self-aligned with said collector.

46. A device as recited in claim 42, comprising:

said base having a ledge;

a first base contact formed on said ledge self-aligned with said emitter.

47. A device as recited in claim 46, comprising:

said base having ledges on opposing sides;

said first base contact formed from a front side of said device;

a second base contact formed opposing said first base contact on said ledge self-aligned with said collector and formed from a back side of said device.

48. A device as recited in claim 42, comprising:

said collector having a width less than a width of said base and greater than a width of said emitter.

49. A device as recited in claim 42, wherein:

said device is a heterojunction bipolar transistor.

50. A device as recited in claim 42, comprising:

said base layer having a lower ledge and an upper ledge;

a first base contact formed on said upper ledge; and

a second base contact formed on said lower ledge.

51. A device as recited in claim 40, wherein:

said first active region is a heterojunction field effect device source region;

said second active region is a heterojunction field effect device drain region; and

said third region is a heterojunction field effect device channel region.